METHOD FOR REDUCING SWITCHING ACTIVITY DURING A SCAN OPERATION WITH LIMITED IMPACT ON THE TEST COVERAGE OF AN INTEGRATED CIRCUIT

Abstract of the Disclosure

A method for reducing the switching activity during both scan-in and scan-out operations of an integrated circuit with reduced detrimental effect on test pattern effectiveness and test time is described. The method makes use of a sample set of patterns to determine the probabilities of same and opposite relationships between stimulus and result values, and uses these probabilities to determine memory element pair compatibilities. Scan chains are ordered preferentially by connecting adjacently compatible memory elements, and inversions are inserted between selected memory element pairs based on those probabilities. Unspecified stimulus bits are filled in to reduce the switching activity based on the scan chain ordering and inversions.